METHOD FOR ADAPTIVE CRITICAL PATH DELAY ESTIMATION DURING TIMING-DRIVEN PLACEMENT FOR HIERARCHICAL PROGRAMMABLE LOGIC DEVICES

ABSTRACT

Provided is a method for estimating delay data comprising receiving an electronic representation of a source electronic design, estimating the criticality of connections which have not yet been placed across a boundary based on statistical data received from at least one other design and revising the design in a manner that biases the design towards a state in which connections with the highest criticality have their delays minimized. A statistical estimate is generated for uncut connections on a path in a partially placed source design comprising receiving at least one source design, partitioning the design, and generating statistical data corresponding to each type of partitioning cut.